REMARKS

The Examiner's Action mailed on June 2, 2004, has been received and its contents carefully considered.

In this Amendment, Applicant has editorially amended the specification, submitted a drawing amendment to Fig. 1, and amended various ones of the claims. Claims 1-20 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Figure 1 has been amended to indicate the leader line of reference number 4 identifying the surface protective film, and not the first insulating layer, as originally submitted. Revised Formal Drawings which incorporate this change are attached hereto.

With respect to the rejection of applicant's claims 1, 4, 11, 14, 17 and 20 over U.S. Pat. No. 6,181,569 to *Chakravorty* in view of U.S. Pat. No. 6,621,154 to *Satoh et al.*, Applicant submits the current amendments to independent claims 1, 11 and 17 provide patentable recitations over the recited prior art.

Chakravorty teaches that "metal in the form of bumps 311-1 are deposited over UBM layer 310," (see Fig. 5a), and "(o)nce the metal bumps 311-1 have been deposited, the portions of the UBM layer 310 that are not covered by bumps 311-1 are removed by (an) etching process." (Column 8, lines 58-66.) "Thus, the UBM layer 310 is left in place only underneath the metal bumps (311-1)." (Column 9, lines 4-5.)

The instant invention discloses wiring layers having bump electrodes formed within depressed portions of the wiring layers, wherein the wiring layers "electrically connect to the corresponding wiring patterns." (Page 5, lines 7-14.)

Applicant's amended claims 1, 11 and 17 further clarify this distinction over the prior art as demonstrated by the following excerpts:

Claim 1, "each of said layers of said wiring ~~each~~ having depressed portions located at via holes formed in said insulating layers, said depressed portions being connected to the lowermost layer of said wiring or said electrode pads, and having flat portions located on said insulating layers and serving as lateral conductors to other electrical connections on said insulating layers;....

Claim 11, "a plurality of redistribution wirings which are formed over the main surface and which are formed at different levels, wherein the redistribution wiring at a lowermost level is connected to the electrode pad, wherein the redistribution wiring at an uppermost level is disposed on the insulating layer and has a depressed portion to which the redistribution wiring at the lowermost level is connected, and flat portions located on said insulating layers and serving as lateral conductors to other electrical connections on said insulating layers;....

Claim 17, "a plurality of redistribution wirings which are formed at different levels, the redistribution wiring at each level being formed on a surface and the via hole of a corresponding insulating layer, wherein the redistribution wiring at a lowermost level is connected to the electrode pad, wherein the redistribution wiring at an uppermost level has a depressed portion located at the via hole

defined by the insulating layer at the uppermost level and is connected to the redistribution wiring of the lowermost level at the via hole, and has flat portions located on said insulating layers and serving as lateral conductors to other electrical connections on said insulating layers;....

The inclusion of "flat portions" located on the insulating layers functioning as lateral conductors to other electrical connections on said insulating layers clearly distinguishes Applicant's amended claims over the teaching of *Chakravorty*. *Chakravorty* definitively states that the UBM layer used to receive the metal conductive bumps is entirely removed by an etching process but for the portion directly under the metal bumps, i.e. all of the flat portions which could serve as lateral conductors are removed. (Column 8, lines 58-66.) It is clear from the teaching of *Chakravorty* that the sole structure and corresponding function of the UBM layer is to only support the metal bump conductor and to potentially provide for an electrically conductive path only to circuits directly underneath and connected to it.

Similarly, *Satoh* fails to overcome this deficiency. Therefore *Chakravorty* and *Satoh*, either alone or in combination, fail to teach all of Applicant's amended claim recitations.

It is noted with great appreciation that the Examiner's Action considers the subject matter of claims 2, 3, 5-10, 12, 13, 15-16, 18 and 19 as being allowable over the art of record. Moreover, since claims 1, 11 and 17 have been amended to incorporate patentable recitations over the recited prior art, all of the Examiner's

prior art rejections have been rendered moot, and this application has thus been placed into condition for allowance. Such action, and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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